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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/024,303	12/21/2001	Ku-suen Lee	13854-054001	3235

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EXAMINER	
LEUNG, CHRISTINA Y	
ART UNIT	**PAPER NUMBER**
2633	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/024,303	LEE ET AL.	
	Examiner	Art Unit	
	Christina Y. Leung	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) . Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 6, 10, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Handelman et al. (US 2002/0048067 A1) in view of Horikawa et al. ("Photonic switched true time delay beam forming network integrated on silica waveguide circuits," 1995 IEEE MTT-S International Microwave Symposium Digest, May 1995, vol. 1, pp 65-68).

Regarding claims 1, 2, and 18, Handelman et al. disclose a multiple-rate optical time division multiplexing (OTDM) module (Figure 2) comprising:

at least one controllable optical delay element (including optical delay mechanism 165 and multiplexer 170) for introducing at least one prescribed optical delay between a plurality of optical RZ signal streams to facilitate time division multiplexing of the plurality of optical RZ signal streams (page 11, paragraphs [0137]-[0142])

wherein the at least one controllable optical delay element is adapted to controllably introduce a selected one of a plurality of optical signal delays to at least one of the plurality of optical RZ signal streams, whereby the time division multiplexing of the plurality of optical RZ signal stream may be facilitated for a number of different data rates (page 11, paragraphs [0137]-[0142]); page 12, paragraph [0146]).

Examiner notes that Handelman et al. disclose that the optical signal streams are return-to-zero (RZ) streams (page 10, paragraph [0123])

Handelman et al. disclose that the optical delay element controllably introduces a selected one of a plurality of optical signal delays to at least one of the plurality of optical RZ signal streams, and further disclose that it comprises an array of delay elements and may be specifically implemented in various ways (page 11, paragraphs [0139]-[0142]) but they do not specifically disclose that it comprises a switching and combining array. Further regarding claim 1 in particular, they also do not specifically disclose that it is integrated.

However, as Handelman et al. already disclose, various ways of implementing a variable optical delay are known in the art, and Horikawa et al. particularly teach a variable optical delay comprising an integrated controllable optical delay switching and combining array (page 65, Abstract; and page 67, Figure 4 and "Experimental Results").

Regarding claim 2 in particular, Horikawa et al. further teach that the integrated controllable optical delay switching and combining array comprises at least one optical switch (switches SW1-3 as shown in Figure 4); and a plurality of optical delay elements (i.e., optical delay lines as shown in Figure 4).

Regarding claims 1, 2, and 18, it would have been obvious to a person of ordinary skill in the art to use an integrated optical delay switching and combining array as taught by Horikawa et al. as the controllable optical delay element in the system disclosed by Handelman et al. as an engineering design choice of a way to provide the already disclosed variable delay in a compact fashion. Horikawa et al. also further teach that their integrated optical delay switching and

combining array advantageously delays signals with low loss and polarization maintenance (page 65, "Introduction").

Regarding claim 6, Handelman et al. further disclose that the at least one controllable optical delay element comprises m-1 optical delay elements, in the sense that they disclose providing m-1 variable delays on the signal paths. Handelman et al. also disclose the at least one prescribed optical delay comprise m-1 prescribed optical delays, wherein the plurality of optical RZ signal streams comprise m optical RZ signal streams (Figure 2 shows that one of the paths contains no delay).

Regarding claim 10, Handelman et al. disclose that the m-1 prescribed optical delays comprise the set of prescribed optical delays Tj/m where j = [1,..., m-1] and T is a period of the plurality of optical RZ signal streams (page 11, paragraph [0140]).

3. Claims 3-5, and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Handelman et al. in view of Horikawa et al. as applied to claims 1, 2, and 6 above, and further in view of Le Sauze (US 6,690,891 B1).

Regarding claims 4 and 8, Handelman et al. in view of Horikawa et al. describe a system as discussed above with regard to claims 2 and 6 respectively.

Horikawa et al. further teach that the integrated controllable optical delay switching and combining array is arranged in a cascaded configuration, wherein the at least one optical switch comprise one 1:2 optical switch and n-1 2:2 optical switches, and wherein the plurality of optical delay elements comprise 2n optical delay elements. Figure 4 shows an arrangement where n=2; SW2 is the one (n-1) 2:2 optical switch, and the system includes four (2n) optical delay paths.

Horikawa et al. do not further teach a 2:1 combiner. However, Le Sauze et al. teach a variable optical delay arrangement (Figure 2) that is closely related to the one already suggested by Horikawa et al., including one 1:2 optical switch, 2 (n-1, where n=3) 2:2 optical switches, and six (2n, where n=3). They further teach that the combining element 4 at the end of their variable optical delay may comprise either a switch (as in the system taught by Horikawa et al) or a 2:1 combiner (page 4, lines 26-27).

Regarding claims 4 and 8, it would have been obvious to a person of ordinary skill in the art to use an optical delay switching and combining array including a 2:1 combiner as particularly taught by Le Sauze et al. in the system already suggested by Handelman et al. in view of Horikawa et al. as an engineering design choice of a way to controllably provide a variable optical delay. A 2:1 combiner as specifically further suggested by Le Sauze also advantageously eliminates having to provide a control signal to the final switch in the arrangement suggested by Horikawa et al.

Further regarding claim 8, Handelman et al. disclose m-1 delay elements and m RZ streams as discussed above with regard to claim 6, but they do not specifically disclose that m is 2. However, it would be well understood in the art that the system disclosed by Handelman et al. may accommodate various numbers of optical streams as desired by the system's users, including m=2. It would have been obvious to a person of ordinary skill in the art have m=2 in the system described by Handelman et al. in view of Horikawa et al. and Le Sauze et al. as an engineering design choice of number of optical streams. The claimed differences exist not as a result of an attempt by Applicants to solve an unknown problem but merely amount to the selection of expedients known as design choices to one of ordinary skill in the art.

Regarding claims 3, 5, 7, and 9, Handelman et al. in view of Horikawa et al. describe a system as discussed above with regard to claims 2 and 6 respectively. Horikawa et al. do not specifically teach that the optical delay switching and combining array comprises the arrangement recited in claims 3, 5, 7, or 9.

However, Le Sauze et al. teach an optical delay switching and combining array arranged in a parallel configuration (Figure 3) and further comprising:

a 2:1 optical combiner (or an "n:1 optical combiner," where n may equal 2);

a 1:2 optical switch (SW in Figure 3; i.e., a 1:n switch, where n may equal 2); and

a plurality of optical delay elements comprising n=2 optical delay elements (delay circuit A [DCA] and delay circuit B [DCB] in Figure 3) coupled to two outputs of the 1:2 optical switch and coupled to two inputs of the 2:1 combiner.

Note that regarding claims 3, 5, 7, and 9, Le Sauze et al. teach an optical delay switching and combining array as shown in Figure 3, while for claims 4 and 8 discussed above, Le Sauze et al. also teach a different arrangement as shown in Figure 2.

Regarding claims 3, 5, 7, and 9, it would have been obvious to a person of ordinary skill in the art to use an optical delay switching and combining array including a 2:1 combiner, a 1:2 optical switch, and two delay elements coupled between the combiner and switch as particularly taught by Le Sauze et al. in the system already suggested by Handelman et al. in view of Horikawa et al. as an engineering design choice of another way to controllably provide a variable optical delay. Le Sauze et al. also teach that the particular optical delay switching and combining array they teach in Figure 3 advantageously provides controllable variable optical delay in a way that minimizes the reliance on high speed switch elements (column 2, lines 10-29).

Further regarding claims 7 and 9, as similarly discussed with regard to claim 8, Handelman et al. disclose m-1 delay elements and m RZ streams as discussed above with regard to claim 6, but they do not specifically disclose that m is 2. However, it would be well understood in the art that the system disclosed by Handelman et al. may accommodate various numbers of optical streams as desired by the system's users, including m=2. It would have been obvious to a person of ordinary skill in the art have m=2 in the system described by Handelman et al. in view of Horikawa et al. and Le Sauze et al. as an engineering design choice of number of optical streams. The claimed differences exist not as a result of an attempt by Applicants to solve an unknown problem but merely amount to the selection of expedients known as design choices to one of ordinary skill in the art.

4. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Handelman et al. in view of Horikawa et al. as applied to claim 1 above, and further in view of Hofmeister (US 6,091,864 A).

Regarding claim 11, Handelman et al. in view of Horikawa et al. describe a system as discussed above with regard to claim 1. They do not specifically suggest at least one electrode deposited over a portion of a waveguide.

However, it would be well understood in the art that the time division multiplexing system described by Handelman et al. in view of Horikawa et al. is particularly concerned with coordinating a plurality of signals in the time domain. Hofmeister particularly teaches that the phase of a plurality of signals relative to each other can be finely adjusted using an electrode deposited over a waveguide (Figure 10; column 11, lines 52-67; column 12, lines 1-15).

It would have been obvious to a person of ordinary skill in the art to include at least one electrode deposited over a portion of a waveguide as suggested by Hofmeister in the system described by Handelman et al. in view of Horikawa et al. in order to ensure that the time division multiplexed signals are exactly aligned in the time domain and do not inadvertently overlap each other.

Regarding claim 12, Handelman et al. in view of Horikawa et al. describe a system as discussed above with regard to claim 1. They do not specifically suggest a power tap for each of the plurality of optical RZ data streams.

However, Hofmeister also teaches including a power tap for optical data streams in an optical communications system in order to monitor the signals (Figure 13; column 12, lines 48-67; column 13, lines 1-9). It would have been obvious to a person of ordinary skill in the art to include power taps as suggested by Hofmeister for the optical data streams in the system described by Handelman et al. in view of Horikawa et al. in order to monitor the incoming signals and detect faults and anomalies in the signals.

5. Claims 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Handelman et al. in view of Horikawa et al. and Johnson et al. ("Fully stabilized electroabsorption-modulation tunable DBR laser transmitter for long-haul optical communications," IEEE Journal of Selected Topics in Quantum Electronics, Mar/Apr 2001, vol. 7, no. 2, pp. 168-177).

Regarding claims 13-17, as similarly discussed above with regard to claim 1, Handelman et al. disclose a multiple-rate optical time division multiplexing (OTDM) module (Figure 2) comprising:

at least one controllable optical delay element (including optical delay mechanism 165 and multiplexer 170) for introducing at least one prescribed optical delay between a plurality of optical RZ signal streams to facilitate time division multiplexing of the plurality of optical RZ signal streams (page 11, paragraphs [0137]-[0142])

wherein the at least one controllable optical delay element is adapted to controllably introduce a selected one of a plurality of optical signal delays to at least one of the plurality of optical RZ signal streams, whereby the time division multiplexing of the plurality of optical RZ signal stream may be facilitated for a number of different data rates (page 11, paragraphs [0137]-[0142]); page 12, paragraph [0146]).

Examiner notes that Handelman et al. disclose that the optical signal streams are return-to-zero (RZ) streams (page 10, paragraph [0123])

Handelman et al. disclose that the optical delay element controllably introduces a selected one of a plurality of optical signal delays to at least one of the plurality of optical RZ signal streams, and further disclose that it comprises an array of delay elements and may be specifically implemented in various ways (page 11, paragraphs [0139]-[0142]) but they do not specifically disclose that it comprises a switching and combining array. They also do not specifically disclose that the time division multiplexing module is integrated.

However, as Handelman et al. already disclose, various ways of implementing a variable optical delay are known in the art, and Horikawa et al. particularly teach a variable optical delay comprising an integrated controllable optical delay switching and combining array (page 65, Abstract; and page 67, Figure 4 and "Experimental Results").

Regarding claim 13, it would have been obvious to a person of ordinary skill in the art to use an integrated optical delay switching and combining array as taught by Horikawa et al. as the controllable optical delay element in the system disclosed by Handelman et al. as an engineering design choice of a way to provide the already disclosed variable delay in a compact fashion. Horikawa et al. also further teach that their integrated optical delay switching and combining array advantageously delays signals with low loss and polarization maintenance (page 65, "Introduction").

Further regarding claim 13, Handelman et al. further disclose that transceivers (i.e., sources of optical pulses) may be optically connected to the optical time division multiplexing elements and form a single module. Figure 3 shows a switching apparatus including converter unit 205 optically connected to optical converter unit 210; Handelman et al. discloses that the converter unit 205 includes transceivers (page 14, paragraphs [0172]-[0172]) and that the optical converter unit 210 in Figure 3 may comprise the same elements as optical converter unit 105 shown in detail in Figure 2 and thereby include the previously discussed time division multiplexing elements (page 14, paragraph [0175]). Handelman et al. do not specifically disclose that the sources of optical pulses comprises an optical pulse source chip.

However, regarding claim 13 and also claim 14, Johnson et al. teach an optical pulse source (OPS) chip comprising a photodiode; a laser source; an electro-absorption modulator (EAM); and a semiconductor optical amplifier (SOA), wherein the photodiode monitors the optical power of the laser source, and the laser source produces an optical signal for gating by the EAM producing an optical pulse signal, said optical pulse signal amplified by the SOA to produce an amplified optical pulse signal (see Abstract, Figure 1, and page 169, left-side column,

second paragraph). Johnson et al. in particular teach: "It is then necessary to add a photodiode after the SOA, preferably monolithically integrated, in order to provide some means of closed-loop power control....The transmitter is based on a highly integrated InP chip comprising a DBR laser, semiconductor optical amplifier, power monitor, and EA modulator."

Regarding claims 15-17 in particular, Johnson et al. teach that the EAM, the SOA, and the laser source are integrated in the same semiconductor chip, as discussed with regard to claim 14.

Regarding claims 13-17, it would have been obvious to a person of ordinary skill in the art to integrate the integrated multiple-rate optical time division multiplexing chip suggested by Handelman et al. in view of Horikawa et al. with the optical pulse source chip taught by Johnson et al. in order to provide a compact implementation of the transmitting and time division multiplexing elements.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christina Y. Leung whose telephone number is 571-272-3023. The examiner can normally be reached on Monday to Friday, 6:30 to 3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on 571-272-3022. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christina Y Leung

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